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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,576	05/03/2002	Ho-Ming Tong	8317-US-PA	4447

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,576	TONG ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-18 and 20-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-18 and 20-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Amendment dated 06/30/04.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a "redistribution layer on the active surface of the wafer" wherein "an under ball metallurgy (UBM) on a redistribution layer" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 10-18 and 20-31 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

➢ With respect to claim 10, "forming an under ball metallurgy (UBM) on a redistribution layer on the active surface of the wafer" is not supported by specification and figures.

➢ With respect to claim 22, "bonding a plurality of conductive studs onto the UBM by wiring bonding wherein each conductive stud has a top surface and a bottom surface opposite to the top surface, wherein the bottom surface is in contact with the UBM and the top surface is flatten by polishing for coplanarity after the conductive stud is bonded onto the UBM; and partially removing the UBM using the above conductive studs as mask until the active surface wafer is exposed" is not supported by specification and figures.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-5, 10-14, 17-18, 22-27, and 30-31, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram [US 5,903,058] in view of Chakraworty [US 6,181,569] and Kimijima et al. [JP 08-213399].

➢ With respect to claim 1, Akram (figs 1's and col 1-3) substantially discloses the claimed method forming a bump on a wafer, wherein the wafer has an active surface (12, figs 1d, col 2 lines 1-22), and the active surface is provided with a passivation layer (16) and a bonding pad (14) exposed by the passivation layer, the method comprising:

forming an adhesive layer (28, fig 1e, col 2 lines 23-39) on the active surface of the wafer to cover the bonding pad (14) and the passivation layer (16);

forming a barrier layer (30, fig 1e, col 2 lines 23-39) on the adhesive layer;

forming a wettable layer (32, fig 1e, col 2 lines 23-39) on the barrier layer;

forming a photomask (36, fig 1f, col 2 lines 40-44) on the wettable layer (32) by a photolithography process, wherein the photomask exposes a portion of the wettable layer;

removing the exposed wettable and sequentially the barrier layer and the adhesive layer thereunder by etching, until the active surface of the wafer is exposed (fig 1g, col 2 lines 44-47);

removing the photomask (fig 1g, col 2 lines 44-47);

bonding a plurality of conductive studs (42, fig 1h, col 1 lines 10-15, col 2 lines 47-51 & 58-67 and col 3 lines 1-3) onto the wettable layer, wherein the conductive studs are made of a material selected from tin/lead alloy, leadless alloy and pure tin, each conductive stud has a top surface and a bottom surface opposite to the top surface wherein the bottom surface being in contact with the wettable layer; and

performing a reflow process to form a plurality of ball -shaped bumps (42, fig 1h, col 1 lines 10-15 & 57-64, col 2 lines 47-51 & 58-67 and col 3 lines 1-3).

Akram does not expressly teach: bonding the plurality of conductive studs by wire bonding; and each conductive stud has a top surface of the conductive stud being flattened by polishing so that the top surfaces of the conductive studs are coplanar. Instead, Akram teaches bonding the conductive stud onto the wettable layer of UBM by stenciling, electroplating or evaporation.

Wire bonding is a known technique to bond the conductive stud. Moreover, Chakravorty (col 9 lines 11-30) teaches using wire bonding is an equivalent technique to stenciling, electroplating or evaporization for bonding the conductive stud on to the UBM. The methods of Chakravorty are expressly taught for low cost chip fabrication (abstract and title). At the time of invention, it would have been obvious for those skilled in the art to modify process of Arkam by using wire bonding as a known technique to

bond the plurality of the conductive studs on the wettable layer as taught by Chakravorty to reduce cost and because Chakravorty shows using wire bonding is the equivalent technique to the bonding technique of Akram.

In addition, Kimijima et al. teaches flattening the top surface of each conductive stud (20, figs 2a-c, abstract) by polishing so that the top surfaces of the conductive studs are coplanar. Said flattening the top surface of each conductive stud will provide a better control of sizes of the conductive studs (21, providing homogeneous bumps having uniform sizes) in forming ball bumps for interconnection. Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Akram in view of Charkravorty by polishing top surface of each conductive stud as claimed, as taught by Kimijima et al., to provide better size-controlled bumps in the semiconductor device. By doing so, homogeneous bumps with uniform sizes will be formed on the device thereby improving reliable-controlled performance of such device.

➢ With respect to claims 10 and 11, as being best understood, Akram (figs 1's and col 1-3) substantially discloses the claimed method of forming a bump on an active surface of a wafer, the method comprising:

forming an under ball metallurgy UBM (28/30/32, fig 1e, col 2 lines 23-39) on the active surface of the wafer wherein the step of forming the UBM onto the active surface of the wafer comprises: forming an adhesive layer (28) on the active surface of the wafer; forming a barrier layer (30) on the adhesive layer; and forming a wettable layer (32) on the barrier layer;

forming a photomask (36, fig 1f, col 2 lines 40-44) on the UBM by photolithography to partially expose the UBM (28/30/32);

removing the exposed portion of the UBM by etching, until the active surface of the wafer is exposed (fig 1g, col 2 lines 44-47);

removing the photomask (fig 1g);

bonding a plurality of conductive studs (42, fig 1h, col 2 lines 47-51 & 58-67 and col 3 lines 1-6) onto the UBM wherein each conductive stud has a top surface and a bottom surface opposite to the top surface, the bottom surface being in contact with the UBM; and

performing a reflow process to form a plurality of ball-shaped bumps (42, fig 1h, col 1 lines 57-64).

Akram does not expressly teach bonding the plurality of conductive studs by wire bonding and the top surface of each conductive stud being flattened by polishing so that the top surfaces of the conductive studs are coplanar. Instead, Akram teaches bonding the conductive stud onto the wettable layer of UBM by stenciling, electroplating or evaporation.

Wire bonding is a known technique to bond the conductive stud. Moreover, Chakravorty (col 9 lines 11-30) teaches using wire bonding is an equivalent technique to stenciling, electroplating or evaporization for bonding the conductive stud on to the UBM. At the time of invention, it would have been obvious for those skilled in the art to modify process of Arkam by using wire bonding as a known technique to bond the plurality of conductive studs on the UBM as taught by Chakravorty to reduce cost and

because Chakravorty shows using wire bonding is the equivalent technique to the bonding technique of Akram.

In addition, Kimijima et al. teaches flattening the top surface of each conductive stud (20, figs 2a-c, abstract) by polishing so that the top surfaces of the conductive studs are coplanar. Said flattening the top surface of each conductive stud will provide a better control of size of the conductive studs (21, providing homogeneous bumps having uniform sizes) in forming ball bumps for interconnection. Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Akram in view of Charkravorty by polishing the top surface of each conductive stud as being claimed, per taught by Kimijima et al., to provide better size-controlled bumps in the semiconductor device.

➢ With respect to claims 22 and 24, Akram (figs 1's and col 1-3) substantially discloses the claimed method of forming a bump on an active surface of a wafer, the method comprising:

forming a UBM (28/30/32, fig 1e, col 2 lines 23-39) on the active surface of the wafer wherein the step of forming the UBM onto the active surface of the wafer comprises: forming an adhesive layer (28) on the active surface of the wafer; forming a barrier layer (30) on the adhesive layer; and forming a wettable layer (32) on the barrier layer;

partially removing the UBM, until the active surface of the wafer is exposed (fig 1g, col 2 lines 44-47); and

bonding a plurality of conductive studs (42, fig 1h, col 2 lines 47-51 & 58-67 and col 3 lines 1-6) onto the UBM wherein each conductive stud has a top surface and a bottom surface opposite to the top surface, the bottom surface being in contact with the UBM.

Akram does not expressly teach bonding the plurality of conductive studs by wire bonding and the top surface of each conductive stud being flattened by polishing for coplanarity after the conductive stud is bonded onto the UBM. Akram teaches bonding the plurality of conductive studs onto the UBM by stenciling, electroplating or evaporation.

However, wire bonding is a known technique to bond the conductive stud. Moreover, Chakravorty (col 9 lines 11-30) teaches using wire bonding is an equivalent technique to stenciling, electroplating or evaporization for bonding the conductive stud on to the UBM. At the time of invention, it would have been obvious for those skilled in the art to modify process of Arkam by using wire bonding as a known technique to bond the plurality of the conductive studs on the UBM as taught by Chakravorty to reduce cost and because Chakravorty shows using wire bonding is the equivalent technique to the bonding technique of Akram.

In addition, Kimijima et al. teaches flattening the top surface of each conductive stud (20, figs 2a-c, abstract) by polishing for coplanarity after bonding the conductive stud on to the UBM will provide a better control of size of the conductive studs (21, providing homogeneous bumps having uniform sizes) in forming ball bumps for interconnection. Therefore, at the time of invention, it would have been obvious for

those skilled in the art to modify process of Akram in view of Charkravorty by polishing the top surface of each conductive stud as claimed, as taught by Kimijima et al. to provide a better size-controlled bumps in the semiconductor device.

➢ With respect to claims 2, 12 and 25, Akram (col 2 lines 23-39) discloses the adhesive layer (28) is formed of titanium, titanium tungsten alloy, aluminum and chromium.

➢ With respect to claims 3, 13 and 26, Akram (col 2 lines 23-39) discloses the barrier layer (30) is formed of a material selected from a group consisting of nickel vanadium alloy, chromium copper alloy, and nickel.

➢ With respect to claims 4, 14 and 27, Akram (col 2 lines 23-39) discloses the wettable (32) layer is formed of a material selected from a group consisting of copper, palladium, and gold.

➢ With respect to claims 5, 18 and 31, the claimed range of lead percentage of the conductive stud is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller* 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious.

> Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art..:such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.

See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

➢ With respect to claims 17 and 30, Akram (col 2 lines 58-67 and col 3 lines 1-3) discloses the conductive stud (42) is formed of tin lead alloy.

➢ With respect to claim 23, Akram substantially discloses the claimed method including reflowing the conductive stud to form the shape of ball for the solder ball (42). Akram is silent about the sequence of the reflowing process being after bonding the conductive stud onto the UBM. However, selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946). Moreover, reflowing the conductive stud to form the shape of ball for bump interconnection after bonding the conductive stud onto the UBM is a known technique of forming bump of solder ball in a semiconductor device. See Chakravorty and Kimijima et al. as evidences that show reflowing the conductive stud to shape the bump of ball after bonding the conductive stud on the UBM. At the time of invention, it would have been obvious for those skilled in the art to the known technique of performing reflowing process after bonding the conductive stud onto the bump, as being claimed, in the process of Akram in view of Chakravorty and Kimijima to form bump of ball-shaped for interconnection of the semiconductor device.

2. Claims 6, 8-9, 15-16, 20-21, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Chakravorty and Kimijima et al. as applied to claims 1, 10 and 22 above, and further in view of Hosaka [US 6,475,897].

➢ With respect to claims 6, 15-16 and 28-29, leadless alloy, tin copper alloy, tin silver alloy, tin magnesium alloy, tin zinc alloy, indium silver alloy, tin bismuth alloy, tin indium alloy, bismuth indium and tin are known materials of conductive stud for forming ball bump interconnection. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co., Inc. v. Interchemical Corp.* , 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." 65 USPQ at 301.). See Hosaka as evidence that shows a usage of claimed material for forming the conductive stud.

➢ With respect to claims 8-9 and 20-21, Akram in view of Chakravorty and Kimijima et al. substantially discloses the claimed method including wire bonding the conductive stud on the wettable layer of the UBM. Akram in view of Chakravorty and Kimijina et al. does not expressly teach bonding the conductive stud onto the UBM/ wettable layer of UBM by: providing a wire; melting one tip end of the wire to form a ball; pressing the ball onto the wettable layer wherein the ball being press onto the wettable layer while applying ultrasonic wave; and separating the ball from the wire to form the conductive stud on the wettable layer.

However, such steps of providing the wire, melting to form the ball, pressing the ball while applying ultrasonic wave and separating the ball from the wire are basis steps of wire bonding technique. See Hosaka as evidence that teaches using the wire bonding technique by providing a wire, melting one tip of the wire to form a ball,

pressing the ball onto a surface where the ball being needed to be bonded to while applying ultrasonic wave, and separating the ball from the wire to form the conductive stud.

Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Hosaka, to use the claimed steps of providing the wire, melting the tip of the wire to form the ball, pressing the ball onto the wettable layer while applying ultrasonic wave and separate the ball from the wire in the process of Akram in view of Chakravorty and Kimijima et al. to bond the conductive stud onto the UBM/the wettable layer of the UBM in a semiconductor device.

Response to Arguments

3. Applicant's arguments filed 06/30/04 have been fully considered but they are not persuasive.

In regarding to Applicant's argument on pages 9-10, Applicant argues that claimed invention can not be obvious over Akram in view of Charkraworty and Kimijima et al because no motivation is equitably provided for one skilled in the art to modify Akram's method by using both teaching from Charkraworty and Kimhima. According to Applicant, it is neither necessary nor reasonable to incoporate Kimijima's polishing process for solving problems arisen from using plating into Arkam's method modified with Charkraworty's wire bonding technique. The hindsight rationalization is contrary to the teachings of Kimijima which thus teaches against the proposed combination.

The argument is not persuasive because Examiner incoporates Kimijima's polishing process into Akram's method modified with Charkraworty's wire bonding technique is to form conductive studs with homogenesous bumps having uniform sizes for better reliable-control device NOT because Kimijima uses the plating process for solders. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-

1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanhha Pham

C. Chaudhari

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